WHAT IS CLAIMED IS:

1. A polished semiconductor wafer having a front surface and a back surface and an edge R, said edge R being located at a distance of a radius from a center of the semiconductor wafer, forms a periphery of the semiconductor wafer and is part of a profiled boundary of the semiconductor wafer, wherein a maximum deviation of flatness of the back surface from an ideal plane in a range between R-6 mm and R-1 mm of the back surface is 0.7 μm or less.

2. The semiconductor wafer as claimed in claim 1, wherein the maximum deviation of the flatness of the back surface from the ideal plane in the range between R-6 mm and R-1 mm of the back surface is 0.5 μm or less.

3. The semiconductor wafer as claimed in claim 1, wherein the front surface is formed by an epitaxially deposited layer.

4. A process for producing a polished semiconductor wafer, comprising:

treating the semiconductor wafer with a liquid etchant at least once, the etchant flowing onto a boundary of the semiconductor wafer during the step of treating; and

polishing at least a front surface of the semiconductor wafer at least once;

wherein the boundary of the semiconductor wafer which faces the flow of etchant is at least partially shielded from being struck directly by the etchant, and wherein the boundary of the semiconductor wafer is shielded along a distance which extends in a direction of a thickness d of the semiconductor wafer and is at least d + 100 μm long.

5. An arrangement comprising a semiconductor wafer and a shield which is positioned in front of a boundary of the semiconductor wafer and at least partially shields the boundary of the semiconductor wafer from a liquid etchant flowing onto the boundary, the arrangement having the following features:

(1) the boundary of the semiconductor wafer is provided with a profile which extends from an inner profile end E, over a length ρ, to an edge R of the semiconductor wafer,

(2) the edge is located at a distance of a radius from a center of the semiconductor wafer and forms a periphery of the semiconductor wafer,

(3) the shield has a border S which is closest to the boundary of the semiconductor wafer and is at a distance Δ from the inner profile end E and a border lying furthest from the boundary of the semiconductor wafer, and

(4) the shield shielding the boundary of the semiconductor wafer which faces the flow of etchant along a distance which extends in a direction of a thickness d of the semiconductor wafer is at least d + 100 μm long.

6. The arrangement as claimed in claim 5, wherein the distance Δ is at most 10 mm.

7. The arrangement as claimed in claim 5, wherein the border S has a recess which extends down to a depth γ to a base G of the recess, and the boundary of the semiconductor wafer extends into the recess.

8. The arrangement as claimed in claim 5, wherein the border of the shield which is furthest from the boundary of the semiconductor wafer is rounded.

9. The arrangement as claimed in claim 5, wherein the shield has a body which is tapered toward at least one of the borders of the shield.